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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,602	07/05/2005	Hong-Sick Park	8071-152T	7109

7590 09/13/2006

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EXAMINER	
MULPURI, SAVITRI	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/516,602	PARK ET AL.	
	Examiner	Art Unit	
	Savitri Mulpuri	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/30/2006.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) -22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the applicant's communication filed on 6/30/2006,amending all independent claims and adding new claims 14-22.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9 –13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chae (US 6,919,931) in combination with Kelly et al(US 6,524,663) and Kydd et al (5,882,722)

Chae teaches a method of manufacturing a thin film transistor array panel, the method comprising:

Forming a gate wire on an insulating substrate "22", the gate wire including a gate line "13", a gate electrode"26", and a gate pad"41";

With respect to claims 4-9, sequentially depositing agate insulating layer ""51", an amorphous silicon layer "53", and ohmic contact layer"55" on the gate wire;

Patterning the ohmic contact layer and the amorphous layer by photolithography;

forming a data wire on the ohmic contact layer, and the adapt wire including source and drain electrodes "28,30", a data line "15" , data pad (not shown);

forming a protective layer "57"on the data wire, the protective layer having a first contact hole "59" exposing the drain electrode, a second contact hole exposing t he gate pad "61"and a third contact hole exposing the data pad (not shown) and;

forming pixel electrode"17", a subsidiary gate pad or transparent pad electrode "43" on gate pad "41", add subsidiary data pad or transparent pad electrode (not shown) on data pad on the protective layer, the pixel electrode being connected to the drain electrode through first contact hole, the subsidiary gate pad being connected to the gate pad through the second contact hole, the subsidiary data pad being connected to the data pad through the third contact hole (see fig 22,3 4A-5 and related description).

With respect to claim 9 Chae also teaches forming protective layer with prominent and depressed portions

Chae does not teach forming an organometallic layer by coating a photosensitive organometallic complex; placing a photomask over the oragnometallic layer such that a predetermined region of the oragnometallic is exposed; exposing the organometallic layer to the light through a photomask; and developing the organometallic layer.

Kelly et al teaches a method of forming a metal pattern for integrated circuits comprising: forming an organ metallic layer by coating a photosensitive organometallic complex; exposing the organometallic layer to light through a photomask; and forming a metal a pattern by developing the organometallic layer(see abstract and col1, lines 46-54). Kelly further teaches making integrated circuits by forming metallization by using organic metal compounds, wherein metals includes Cu Ni, gold , or any other

suitable metals (see col. 8, lines 47-50; col. 9, lines 46-49), which inherently includes aluminum because Al is very old and popular metal for metallization in integrated circuits. It would have been obvious to one of ordinary skill in the art to form metal pattern in the invention of Chae by forming organometallic layer by coating a photosensitive organometallic complex and exposing the organometallic layer to light through photomask and developing and forming a metal pattern by developing the organometallic layer because such process is electroless plating and gives good quality result and metal pattern can be formed on the insulator or on the semiconductor or on the conductors(see col. 1, lines 35-45). Chae in view of Kelly would result the same structure as the structure recited in claims 10-13 (see fig. 2, -4 and related description).

With respect to claims 1-13, 14,17,19,21 neither Chae nor Kelly teach organic material containing Ag.

Kydd et al (5,882,722) teaches metal organic decomposition(MOD) by using organic metallic complex containing silver to form metal as a contact on semiconductor materials(abstract, col.3, lines 34-39,col. 4, lines 10-21,.col.10, lines 25-40), structure in co.8, all examples. It would have been obvious to one of ordinary skill in the art to form silver alternative disclosed materials such Pd, Pt Ag etc., because both Ag and Pd transitional metals and functionally equivalent.

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art teaches forming thin film transistor array panels.

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m. to 4.30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt, can be reached on 571-272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Savitri Mulpuri
Primary Examiner
Art Unit 2812